PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	10/736,386	Conf. No.:	6227
Filed:	December 15, 2003		
Title:	**METHOD FOR CALCULATING HIGH-RESOLUTION WAFER PARAMETER PROFILES**		
Inventors:	Bruce Whitefield et al.		
Art Unit:	2128		
Examiner:	Hugh M. Jones		
Atty. Ref:	03-1345		

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-captioned patent application is respectfully submitted to the Honorable Board of Patent Appeals and Interferences after final rejection by Examiner Hugh M. Jones, Group Art Unit 2128, refusing allowance of the claims as presented and amended in the above-captioned patent application. A copy of the claims in issue is included herewith in the Appendix.

The present Appeal Brief is in furtherance of the Notice of Appeal filed in this case on May 12, 2009.

The Commissioner is authorized to charge payment of any fee required in connection with this appeal to Deposit Account No. 12-2252.

This brief contains the following items under the following headings and in the order set forth below (37 CFR 41.37):

i. Real party in interest;

ii. Related appeals and interferences;

iii. Status of claims;

iv. Status of the amendments;

v. Summary of the claimed subject matter;

vi. Grounds of rejection to be reviewed on appeal;

vii. Argument;

viii. Claims appendix;

ix. Evidence appendix; and

x. Related proceedings appendix.

The final page of this brief bears the attorney's signature.

I. REAL PARTY IN INTEREST

The real party in interest is the Assignee of the present patent application, LSI Corporation, a corporation organized and existing under the laws of the State of Delaware, having its principal place of business at 1621 Barber Lane, Milpitas, California 95035.

II. RELATED APPEALS AND INTERFERENCES

There are no other pending, related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS

There are twenty-one (21) claims pending in the present application, claims 1-21, which stand finally rejected and are on appeal.

IV. STATUS OF THE AMENDMENTS

The claims were amended on September 4, 2008 in response to the Office Action mailed July 7, 2008. The Examiner then issued an Advisory Action on September 11, 2008. Applicant filed a Request for Continued Examination and Response to Advisory Action on October 7, 2008. The Amendment filed on September 4, 2008 was considered by the Examiner and the Examiner issued another Office Action on October 20, 2008, maintaining the rejection of each of the pending claims. Applicant submitted arguments in response to the October 20, 2008 Office Action on January 20, 2009, and the Examiner then issued another Office Action on March 5, 2009, maintaining the rejection of each of the pending claims. Applicant filed a Notice of Appeal and Pre-Appeal Brief Request for Review on May 12, 2009.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention generally a method for calculating high-resolution wafer parameter profiles. The present invention provides a method to utilize data from many different die sizes and products so that highly detailed wafer profiles can be generated that have an improved signal to noise ratio and spatial resolution. Instead of being limited to single die size like normal wafer maps, this method takes advantage of multiple die sizes and their variation in placement on the wafer to increase the information available about the wafer patterns (see lines 5-11 of page 6 of the specification).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-21 are pending in the application. Claims 1-2 and 5-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent No. 5,864,394 (Jordan, III et al.), claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Jordan, III et al. in view of United States Patent No. 6,885,950 (Misutake et al.), and claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Jordan, III et al. in view of United States Patent No. 7,065,239 (Maaya et al.).

VII. ARGUMENT

In response to the third Office Action which was mailed on October 20, 2008, Applicant argued that the claims are patentable over the references cited by the Examiner. Although the Examiner maintained his rejection of the claims in the Final Office Action which was mailed on March 5, 2009, Applicant requests reconsideration of the following arguments.

Claim 1 specifically claims, among other things, the step of defining an appropriate product/device input dataset for a plurality of different die sizes and products, wherein the dataset comprises information relating to the size of each die in two directions as well as the location of at least one of the corners of each die. Claim 1 also claims using this dataset to generate a table of lots and wafer of a product/device with a virtual die coordinate for each die and a corresponding value.

In the Office Action, the Examiner asserted that Figure 7 of Jordan, III et al. discloses "information relating to the size of each die in two directions as well as the location of at least one of the corners of each die." While this may be true, Applicant is not merely claiming that. Applicant is claiming the step of defining an appropriate product/device input dataset for a plurality of different die sizes and products (wherein the dataset comprises physical correlation reference points comprising information relating to the size of each die in two directions as well as the location of at least one of the corners of each die), and collecting a die level yield bin dataset for one of the products/devices by using the product/device input dataset to generate a table of data for the lots and wafers of said one of the products/devices with a virtual die coordinate for each die and a corresponding value.

Figure 7 of Jordan, III et al. merely illustrates a wafer, and the fact that it includes a repeating pattern (see col. 12, lines 37-43). Figure 7 of Jordan, III et al. discloses a plurality of dies on a wafer and that the dies have corners, etc., but does not disclose providing a dataset which comprises information relating to the size of each die in two directions as well as the location of at least one of the corners of each die.

Applicant respectfully submits that Jordan, III et al. fails to disclose defining a dataset as

recited in claim 1 (i.e., one which comprises physical correlation reference points comprising information relating to the size of each die in two directions as well as the location of at least one of the corners of each die), let alone using the dataset as recited in claim 1 (i.e., to generate a table of data for the lots and wafers of said one of the products/devices with a virtual die coordinate for each die and a corresponding value).

Additionally, Applicant respectfully submits that Jordan, III et al. is very different from the present invention. Jordan, III et al. deals with scanning for anomalies. That is not what the present invention is directed to. In contrast, the present invention is directed to calculating high-resolution wafer parameter profiles.

Figure 7 of Jordan, III et al. merely illustrates a wafer, and the fact that it includes a plurality of dies on a wafer and that the dies have corners, etc. However, no where is it disclosed or suggested to provide a dataset which comprises information relating to the size of each die in two directions as well as the location of at least one of the corners of each die, and using this dataset to generate a table of data for the lots and wafers of said one of the products/devices with a virtual die coordinate for each die and a corresponding value.

Applicant respectfully submits that the pending claims are patentable over the cited references and are allowable. In view of the above remarks, Applicant respectfully requests that the present application be passed to issuance.

VIII. CLAIMS APPENDIX

1. A method for calculating high-resolution wafer parameter profiles comprising the steps of:

a) defining an appropriate product/device input dataset for a plurality of different die sizes and products, wherein the dataset comprises physical correlation reference points comprising information relating to the size of each die in two directions as well as the location of at least one of the corners of each die;

b) collecting a die level yield bin dataset for one of the products/devices defined in step (a) by using the product/device input dataset to generate a table of data for the lots and wafers of said one of the products/devices with a virtual die coordinate for each die and a corresponding value;

c) calculating a single composite value for each said virtual die coordinate;

d) defining where on a virtual die it is desired to assign a composite value;

e) calculating physical coordinates for each die value using the corresponding virtual coordinate and a physical translation key;

f) repeating steps (b), (c), (d) and (e) for each of said die sizes and products defined in step (a);

g) merging the data from a plurality of files into one file;

h) defining a grid;

i) creating a table with all possible grid coordinates that would fit on a production wafer;

j) defining a smoothing algorithm;

k) calculating the smoothed value for each point on the grid from the combined data; and

l) plotting a wafer profile.

2. A method as defined in claim 1, further including the step of normalizing the composite die values so that they are mergeable with values from the other products.

3. A method as defined in claim 2, wherein a Poisson Defect Density normalizing algorithm is used to perform the step of normalizing the composite die values so that they are mergeable with values from the other products.

4. A method as defined in claim 2, wherein a max-min scaling normalizing algorithm is used to perform the step of normalizing the composite die values so that they are mergeable with values from the other products.

5. A method as defined in claim 1, wherein said appropriate product/device input dataset of step (a) are defined by a variety of devices with die level data and different die sizes.

6. A method as defined in claim 1, wherein said appropriate product/device input dataset of step (a) are defined by products/devices which represent the same process flow to be modeled.

7. A method as defined in claim 1, wherein said appropriate product/device input dataset of step (a) are defined by a number of lots from each device to calculate an average result value for each die.

8. A method as defined in claim 1, wherein said appropriate product/device input dataset of step (a) are defined by die size for each device.

9. A method as defined in claim 1, wherein said appropriate product/device input dataset of step (a) are defined by at least one reference physical correlation point between a specific virtual coordinate and an actual physical location on the wafer.

10. A method as defined in claim 1, wherein said calculated single composite value for each die coordinate from step (c) is an average of the data from all the individual lots and wafers corresponding to the die site.

11. A method as defined in claim 1, wherein said calculated single composite value for each die coordinate from step (c) is a max of the data from all the individual lots and wafers corresponding to the die site.

12. A method as defined in claim 1, wherein said calculated single composite value for each die coordinate from step (c) is a sum of the data from all the individual lots and wafers corresponding to the die site.

13. A method as defined in claim 1, wherein said calculated single composite value for each die coordinate from step (e) is a percentage of the data from all the individual lots and wafers corresponding die site.

14. A method as defined in claim 1, wherein said composite value from step (d) is assigned to a corner of the die nearest an edge of the wafer.

15. A method as defined in claim 1, wherein said composite value from step (d) is assigned to a corner of the die nearest a center of the wafer.

16. A method as defined in claim 1, wherein said composite value from step (d) is assigned from a center of the die.

17. A method as defined in claim 1, wherein a Cartesian coordinate system is used to calculate physical coordinates from step (e).

18. A method as defined in claim 1, wherein a polar coordinate system is used to calculate physical coordinates from step (e).

19. A method as defined in claim 1, wherein the wafer profile is scaled, in accordance with step (l), in equal increments of a range of values.

20. A method as defined in claim 1, wherein the wafer profile is scaled, in accordance with step (l), in equal percentiles of the data.

21. A method as defined in claim 1, wherein the wafer profile is plotted, in accordance with step (l), to show a three-dimensional contour map of the data.

IX. EVIDENCE APPENDIX

There was no evidence presented during prosecution.

X. RELATED PROCEEDINGS APPENDIX

There are no other pending, related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

CONCLUSION

In summary, the prior art cited by the Examiner does not anticipate or render obvious the claims of the present invention because it does not disclose or suggest calculating high-resolution wafer parameter profiles.

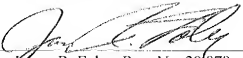
Therefore, Appellant respectfully requests that the Board:

1. Direct the Examiner to withdraw the rejection of claims 1-2 and 5-21 in the application under 35 U.S.C. §102(b).
2. Direct the Examiner to withdraw the rejection of claims 3 and 4 in the application under 35 U.S.C. §103(a).
3. Direct the Examiner to proceed with issuance of the present application.

This Appeal Brief is respectfully submitted by:

Attorneys for Applicant/Appellant

Date: June 15, 2009

By: 

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